Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 10007099 -1 #12

CB — 5/5/04

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Blaine D. Gaither et al **Confirmation No.:** 2685

Application No.: 09/704176 **Examiner:** Elmore, Stephen C

Filing Date: Oct 31, 2000 **Group Art Unit:** 2186

Title: Cache Coherence Protocol For A Multiple Bus Multiprocessor System

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in **triplicate** is the Appeal Brief in this application with respect to the Notice of Appeal filed on 04/29/2004.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $330.00.

05/05/2004 CBARNES1 00000005 082025 09704176

01 FC:1402 330.00 DA

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$110.00
( )	two months	$420.00
( )	three months	$950.00
( )	four months	$1480.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $330.00. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

( ) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit:_____

OR

(X) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (703) 872-9306 on 04/29/2004

Number of pages: 31

Typed Name: Donna M Kraft

Signature: Donna M Kraft

Respectfully submitted,

Blaine D. Gaither et al

By A. W. Winfield

Augustus W Winfield

Attorney/Agent for Applicant(s)
Reg. No. 34,046

Date: 04/29/2004

Telephone No.: 970 898 3884

OFFICIAL

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Mail Stop 35
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 10007099-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Blaine D. Gaither & Russ W. Herrell	Confirmation No. 2685
Serial No.:	09/704,176	Examiner: Elmore, Stephen C.
Filing Date:	10/31/2000	Group Art Unit: 2186

Title: CACHE COHERENCE PROTOCOL FOR A MULTIPLE BUS MICROPROCESSOR SYSTEM

THE ASSISTANT COMMISSIONER OF PATENTS
Washington, D.C. 20231

Sir:

BRIEF ON APPEAL

INTRODUCTION

Pursuant to the provisions of 37 CFR § 1.191 *et seq.*, applicants hereby appeal to the Board of Patent Appeals and Interferences (the "Board") from the examiner's final rejection dated 01/29/2004. A notice of appeal was timely filed concurrently with this Brief on Appeal on April 29, 2004, in accordance with 37 CFR § 1.8. This brief on appeal is being filed in triplicate (37 CFR § 1.192(a)) and is accompanied by the requisite fee (37 CFR 1.192(a) and 1.17(c)).

REAL PARTY IN INTEREST

The entire interest in the present application has been assigned to Hewlett-Packard Development Company, L.P., as recorded at reel 014061, frame 0492.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1, 5, 11, and 12 have been finally rejected.

Claims 2, 4, and 6 are objected to.

Claims 1, 5, 11, and 12 are on appeal.

STATUS OF AMENDMENTS

All previous amendments have been entered. There are no after-final amendments.

SUMMARY OF INVENTION

The invention relates generally to computer systems, and more specifically to cache memory systems, and still more specifically to coherency protocols for cache memory systems in multiprocessor computer systems. In a computer system in accordance with the invention, cached lines are either owned (potentially modifiable) or shared. The computer system maintains a list of address references, for example tags, called a Global Ownership Tag List (GOTL), for all the cache lines in the system for which a cache has ownership. *(See, figure 3A, 304; figure 3B, 312; figure 4A, 404; and figure 4B, 410).* For each address reference in the GOTL, the corresponding line may be dirty (modified), or may be only potentially dirty (modifiable). *(See page 6, line 18, through page 7, line 20).*

There may be one central GOTL. *(See, for example, figures 3B and 4B).* Alternatively, the GOTL may be distributed, so that every device that can request a copy of memory data (for example, processors, bus bridges, and snoop filters) maintains a local identical copy of the GOTL. *(See, for example, figures 3A and 4A) (See also, page 7, lines*

15-20; page 8, line 9, through page 9, line 6). The number of tags in a GOTL can be much smaller than the number of lines in all the caches in the system. For a limited size GOTL, an existing tag may need to be evicted to make room for a new tag. *(See, for example, page 10, lines 11-26)*.

Claim 1 specifies a plurality of memory caches *(figures 3A and 3B, 302; figures 4A and 4B, 406)*; a list *(figure 3A, 304; figure 3B, 312; figure 4A, 404; figure 4B, 410)* containing; an address reference for every line in the plurality of memory caches for which a corresponding line in memory may not be identical; and an indicator of which cache owns each line; and the list not containing; address references for lines that are shared or uncached; and data corresponding to the address references *(see, for example, page 7, line 21, through page 8, line 4; see also, page 10, lines 1-10)*.

Claim 5, dependent on claim 1, further specifies that the list comprises a single list shared by all devices in the computer system *(figures 3B and 4B; page 7, line 15)*.

Claim 11 specifies entering into a list, an address reference for all lines that are owned; not entering into the list address references for lines that are shared or uncached; updating the list only when ownership of a line changes; *(page 7, line 21, through page 8, line 4;* page 9, *lines 12-14; page 10, lines 1-10)* and, removing an address reference to a line, from the list, when the line has remained in the list for longer than a specified time *(page 10, lines 11-26)*.

Claim 12 specifies entering into a list, an address reference for all lines that are owned; not entering into the list address references for lines that are shared or uncached; updating the list only when ownership of a line changes; *(page 7, line 21, through page 8, line 4; page 9, lines 12-14; page 10, lines 1-10)* and removing an address reference to a line, from the list, even when the list is not full, to help prevent the list from filling *(page 10, lines 11-26)*.

ISSUES

1. Whether claims 11 and 12 are unpatentable under 35 U.S.C. § 112, first paragraph, as not being enabled by the specification.

2. Whether claims 1 and 5 are unpatentable under 35 U.S.C. § 102(b) as anticipated by U.S. Patent Number 5,655,103 (Cheng *et al.*)

GROUPING OF CLAIMS

For purposes of this appeal, each of claims 1 and 12 stands on its own, as discussed in the following Argument section.

For purposes of this appeal, claim 5 stands or falls together with claim 1.

For purposes of this appeal, claim 11 stands or falls together with claim 12.

ARGUMENT

Outline

I. Summary of the brief on appeal.
II. Summary of the requirements for enablement under 35 U.S.C. § 112, first paragraph, as applied to issue 1.
III. Discussion of claim 12 in relation to issue 1.
IV. Summary of the requirements for anticipation under 35 U.S.C. § 102.
V. Discussion of claim 1 in light of Cheng *et al.*

I. Summary of the brief on appeal.

1. There is express support in the detailed description section of the application for the disputed element of claim 12.

2. Cheng *et al.* do not teach or suggest a list containing an address reference for every line in the plurality of memory caches for which the corresponding line in memory may not be identical, and the list not containing address references for lines that are shared or uncached.

II. Summary of the requirements for enablement under 35 U.S.C. § 112, first paragraph, as applied to issue 1.

From MPEP 2164: "Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention."

From MPEP 2163 I.B.: "The claims as filed in the original specification are part of the disclosure . . .."

III. Discussion of claim 12 in relation to issue 1.

The examiner asserts that the disclosure does not provide enablement for the element: "updating the list only when ownership of a line changes." In particular, the examiner notes that an address reference may be removed from the list, and that removing an item is included in "updating". If applicant correctly understands the examiner's remarks in paper 10, pages 7 and 8, the examiner is limiting the term "ownership change" to just the case when ownership changes from one cache to another cache.

The element as worded is consistent with the detailed description section of the application. Applicant has defined "ownership" at page 3, lines 1-3. A cache "owns" a line if the cache has permission to modify the line without issuing any further coherency transactions. That is, the line is modified or modifiable. Accordingly, ownership changes if a line state changes from owned (modified or modifiable) to unowned (some state other than modified or modifiable), or if a line state changes to modified or modifiable from other state. Ownership may also change from one cache to another cache. From page 9, lines 12-14: "The only time a GOTL needs to be updated is when a line transitions from owned to shared, from shared to owned, or when ownership changes." If a line state changes from owned to shared, the list is updated by removing the line from the list (ownership changes). If a line changes from shared to owned, the list has to be updated to add the line to the list (ownership changes). If ownership changes from one cache to

another cache, the list has to be updated to identify the ownership change. See also, page 7, line 21, through page 8, line 4. As described in the specification, every update to a GOTL is a result of an ownership change, as specified in claim 12.

In addition, from MPEP 2163 I.B., the cited element, which was submitted as part of claim 7 in the original application as filed, is part of the disclosure, and accordingly is enabled if it contains sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. The element as worded in the claim is, by definition, a disclosed embodiment.

IV. Summary of the requirements for anticipation under 35 U.S.C. § 102.

From MPEP 2131:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

"The elements must be arranged as required by the claim, but . . . identity of terminology is not required." *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990).

V. Discussion of claim 1 in light of Cheng *et al.*

Claim 1 specifies a list containing an address reference for every line in the plurality of memory caches for which the corresponding line in memory may not be identical, and the list not containing address references for lines that are shared or uncached. Cheng *et al.* do not teach or suggest a list containing an address reference for every line in the plurality of memory caches for which the corresponding line in memory may not be identical and the list not containing address references for lines that are shared or uncached.

In Cheng *et al.*, there are two lists: a directory (figure 1, 109) and a dependency table (figure 3, 109). The directory contains address references for lines that are shared or

uncached, and therefore does not satisfy the requirements of claim 1. From column 1, lines 22-26, a typical directory includes references to uncached data located in system memory. There is nothing in Cheng *et al.* that teachs or suggests that the directory in Cheng *et al* is different than the directory described in column 1.

The dependency table does not contain an address reference for every line in the plurality of memory caches for which the corresponding line in memory may not be identical. The dependency table only includes those lines for which there is a Load Miss (column 5, lines 11-14; figure 2, steps 205 and 215). That is, there may be dirty lines owned by one processor that are never requested by another processor, and accordingly, there is never a Load Miss request, and accordingly there is no entry for those lines in the dependency table.

In paper 10, page 4, for the element specifying "a list containing an address reference for every line in the plurality of memory caches for which a corresponding line in memory may not be identical", the examiner cites figure 1, element 109, and column 2, lines 18-21 and 27-31. The cited figure and the first text citation (column 2, lines 18-21) refer to the directory. The second text citation (column 2, lines 27-31) refers to the dependency table, which is a separate list. For the element specifying "a list not containing address references for lines that are shared or uncached", the examiner asserts, without citation to Cheng *et al.*, or without specifying which list (directory or dependency table) in Cheng *et al.*, that the list does not contain address references for lines that are uncached. For a directory, this assertion is expressly contradicted by Cheng *et al.* at column 1, lines 22-26.

CONCLUSION

In view of the above, applicant respectfully requests that the examiner's rejection of claims 1, 5, 11, and 12, be reversed.

Respectfully submitted,

by A. W. Winfield

Augustus W. Winfield

Reg. No. 34,046

April 28, 2004

Fort Collins, CO 80528-9599

(970)-898-3142

CLAIMS ON APPEAL

1. A computer system comprising:

a plurality of memory caches;

a list containing;

an address reference for every line in the plurality of memory caches for which a corresponding line in memory may not be identical; and

an indicator of which cache owns each line; and

the list not containing;

address references for lines that are shared or uncached; and

data corresponding to the address references.

5. The computer system of claim 1, wherein the list comprises a single list shared by all devices in the computer system.

11. A method for maintaining cache coherency in a computer system, comprising:

entering into a list, an address reference for all lines that are owned;

not entering into the list address references for lines that are shared or uncached;

updating the list only when ownership of a line changes; and

removing an address reference to a line, from the list, when the line has remained in the list for longer than a specified time.

12. A method for maintaining cache coherency in a computer system, comprising:

entering into a list, an address reference for all lines that are owned;

not entering into the list address references for lines that are shared or uncached;

updating the list only when ownership of a line changes; and

removing an address reference to a line, from the list, even when the list is not full, to help prevent the list from filling.